

Abstract of the Disclosure

In a computer which translates instructions from a target instruction set to a host instruction set, a method for determining validity of a translation of a target instruction linked to an earlier translation

5 including the steps of testing a memory address of a target instruction to be executed against a copy of the memory address of the target instruction from which a translation of the target instruction was made, executing the translation if the addresses compare, and generating an exception if the addresses do not compare.

10